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10/032,757	12/27/2001	Angela Hui	G0728/2236P	5788

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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 10/032,757
Filing Date: December 27, 2001
Appellant(s): HUI ET AL.

Robert A. Voigt, Jr., reg. No. 47,159
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/12/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences that will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 2 and 3.

Claims 16-19 are allowed.

Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7-15 are withdrawn from consideration as not directed to the elected invention.

Claim 1 is canceled.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows:

A. Are claims 2-3 properly rejected under 35 U.S.C.§ 102(e) as being anticipated by Lien (U.S. Patent No. 6,338,993)?

Appellant's brief presents arguments relating to the rejection of claims 4-6 and 16-19. This issue is no longer applicable since the status of these claims has changed. Claims 16-19 are now allowed and claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(7) Grouping of Claims

The rejection of claims 2 and 3 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,933,730	SUN	8-1999
6,338,993	LIEN	1-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 2 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Lien (US 6338993).

Regarding claim 2, Lien (see, *e.g.*, fig. 7) shows all aspects of the instant invention including a semiconductor device including a core **30** and a periphery **10, 20**, the semiconductor device comprising:

- ✓ A plurality of core gate stacks in the core **30**, each of core gate stacks including a first polysilicon gate **240** and a WSi layer **250** above the first polysilicon gate **240**
- ✓ A plurality of core spacers **400**, each of the core spacers **400** residing along an edge of the core gate stacks
- ✓ A plurality of sources **300** in the core **30**, the sources **300** residing between a portion of the core gate stacks
- ✓ A plurality of periphery gate stacks in the periphery **10, 20**, each of the periphery gate stacks including a second polysilicon gate **231, 232** and a CoSi layer **500** on the second polysilicon gate

Regarding claim 3, Lien (see, *e.g.*, fig. 7) shows each of the periphery gate stacks including an edge, the semiconductor device further comprising a plurality of

periphery spacers **410, 420**, each of the periphery spacers **410,420** residing along an edge of the periphery gate stacks.

(11) Response to Argument

The appellants argue:

> Element 400 in Lien's figure 7 is not a spacer. Lien differently shows that element 400 is a silicon nitride layer deposited over the periphery region (PMOS 10 and NMOS 20 regions) and the core region (memory cell region 30). The silicon nitride layer is used as a protective layer of the core region during a salicide process. Lien further teaches that the silicon nitride layer 400 is etched to form spacers 410, 420 on the periphery region 10, 20. Since Lien discloses etching the nitride layer 400 in the periphery region 10, 20 to form spacers 410, 420 but does not disclose etching the nitride layer 400 on the core region 30 to form spacers, he does not disclose the limitation in claim 2 reciting a plurality of core spacers residing along an edge of the core gate stacks. Thus, Lien does not anticipate claim 2.

The examiner responds:

The appellant's arguments are mainly directed to process aspects of the invention. The claims, however, are directed to a structure not to a process.

In spite of the above, the fact that Lien discloses etching the nitride layer **400** to form spacers **410, 420** on the periphery region **10, 20** and fails to disclose etching the nitride layer **400** to form spacers in the memory region **30** does not oppose the fact that the nitride layer **400** on the core region is also a spacer. To illustrate this point, the examiner submitted in the final Office action mailed 12/3/2003 a response to a similar argument from the appellants. In said Office action, Sun (US 5933730), a teaching reference, was provided to illustrate the fact that there are different types of spacers in the art. In fact, Sun's different spacers **714, 714', 730, 740** are formed in different ways. In figure 9F, for example, Sun shows that spacers **714'** are formed in the core region by etching an oxide layer. However, the spacer **714** in the peripheral region remains untouched by the etching process (see, *e.g.*, col.5/ll.10-24). Similarly, in figure 9K, a spacer **740** in the peripheral region is formed by etching an oxide layer. However, the

spacer **730** in the core region remains untouched by the etching process (see, *e.g.*, col.5/ll.59-64).

In light of the above, the fact that Lien uses etching to form the spacers **410, 420** in the peripheral region **10, 20** and does not use etching to form the spacer **400** in the core region **30** is not evidence that the nitride layer **400** in the core region **30** is not a spacer, as spacers are known in the art.

The appellants have failed to establish the structural differences between the claimed core spacers and those of Lien. As noted before, the appellant's arguments are mainly directed to process aspects of the invention. The claims, however, are directed to a structure not to a process. Any process limitation in the claims is considered only in terms of a necessary resultant structure. The process itself is not at issue. The device claims are not limited to a recited process limitation. The claims, however, even fail to recite any process limitation with respect to the manner in which the core spacers are made. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claims only recitation about the core spacers is that there is a plurality of them, each residing along an edge of the core gate stacks. Lien (see, *e.g.*, fig. 7) clearly shows a plurality of core spacers **400**, with each of the spacers **400** residing along en edge of the core gate stacks.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 4/26/2004 with Mr. Marcos D. Pizarro-Crespo (Patent Examiner), Mr. Olik Chaudhuri (Supervisory Patent Examiner), and Mr. Wael Fahmy (Supervisory Patent Examiner) as the conferees.

Respectfully submitted,

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mdp/MDP
April 28, 2004

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